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4: Combinational Logic I (ETH  
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Boolean Logic \u0026amp; Logic Gates:  
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A = 1 and B = 1, B=1, \! B = 1,  
the latch state is Q = 1, Q=1, Q =  
1, (e) Derive a circuit for the A B  
AB A B latch using four two-input  
NOR \text {NOR}\! NOR gates  
and two inverters. An A B AB\!  
A B latch operates as follows: If A

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Manual  $A=0$ !  $A = 0$  and  $B = 0$ ,  
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Quartus CAD software comes free  
with every copy of the text. The  
CAD software provides automatic  
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Verilog into Field Programmable  
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Manual (CPLDs). Students will be able to try, firsthand, the book's Verilog examples (over 140) and homework problems. Engineers use Quartus CAD for designing, simulating, testing and implementing logic circuits. The version included with this text

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supports all major features of the commercial product and comes with a compiler for the IEEE standard Verilog language.

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and timing of the resulting circuit implement the designs in actual devices (using the school's laboratory facilities) Verilog is a complex language, so it is introduced gradually in the book. Each Verilog feature is presented as it becomes pertinent for the

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