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Viterbi

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Information Theory
And Coding -

Convolutional Codes

Convolutional Code

Encoder|State Table

and State Diagram of

Convolutional Code|

Information Theory

Convolution Encoder-

Input State Transition

Diagram, Trellis

Diagram.

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basics, designing
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Encoding using Time
domain and
Transform Domain
Approaches
Convolutional Codes
States and Code tree
in Digital

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~~I: Encoding~~ How to

draw Trellis diagram

for a given encoder

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Classification,

Realization

~~Convolutional Code,~~

~~Encoder, State~~

~~Diagram, Code Tree,~~

~~Trellis, Viterbi~~

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Problem on

Convolution Encoder.

Viterbi Decoder with

example

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Output (C1W3L03)
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Representation of
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~~Vaishali~~

(2, 1, 1) Convolutional

code | Tree diagram |

Information Theory

and Coding

~~Convolutional Codes~~

~~Introduction | Code~~

~~Rate, Constraint~~

~~Length, Code~~

~~Dimension~~

~~Implementation Of~~

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Convolutional

Encoder And

Implementation of

convolutional encoder

and Viterbi decoder

using VHDL Abstract:

This work focuses on

the realization of

convolutional encoder

and adaptive Viterbi

decoder (AVD) with a

constraint length, K of

3 and a code rate

(k/n) of $1/2$ using field-

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programmable gate
array (FPGA)
technology.

Convolutional

Implementation of
convolutional encoder
and Viterbi ...

Convolutional codes
are non blocking
codes that can be
designed to either
error detecting or
correcting.

Convolution coding

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has been used in communication systems including deep space communication and wireless communication. At the receiver end the original message sequence is obtained from the received data using Viterbi decoder.

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[PDF] Implementation of Convolution Encoder and Viterbi ...
Convolutional codes are employed to implement FEC .It take a single or multi-bit input and generate a matrix of encoded outputs. Figure 2.1.1:Convolutional Encoder of code rate $\frac{1}{2}$. Above shows block diagram of $\frac{1}{2}$

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rate convolutional encoder. Using this let us draw truth table.

Trellis Diagram:

Trellis diagram can be obtained by using above truth table.

Firstly write the

FPGA Design and Implementation of Convolution Encoder and ...

The process of adding

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this redundant information is known as channel coding. Convolutional codes operate on serial data, one or a few bits at a time.

Convolutional encoding with Viterbi decoding is a FEC technique that is particularly suited to a channel in which mainly Additive White

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Gaussian Noise
(AWGN) corrupts the
transmitted signal.

Convolutional

Convolutional And

encoder example |

Convolutional coding

The 1 in the generator
polynomial indicates
the connections and
zero indicates no
connections between
the stage and the
modulo 2 adder. The

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figure below illustrates a simple convolutional coder with $k=1, K=3, n=3, g_1(n) = (1\ 0\ 1), g_2(n) = (1\ 1\ 1), g_3(n) = (0\ 1\ 1)$ and $R=1/2$.

Fig 2.2 Convolutional Encoder.

Implementation of Reconfigurable Convolutional Encoder and ...

Viterbi decoding is the

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Best technique for decoding the convolutional codes. Convolution encoder and Viterbi decoder are widely used in many communication systems due to the excellent error control performance. This work deals with the design and implementation of convolution encoder

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Implementation of Viterbi decoder using Field Programmable Gate Array.

Encoder And

Design and Implementation of Convolutional Encoder and ...

The most important aspect dealt in this paper is the implementation of Convolution encoder

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and Viterbi decoder on FPGA platform by reducing the area and henceforth improving the speed performances. In general digital/wireless communication systems were designed on Digital Signal Processors (DSPs).

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An Efficient FPGA
Implementation of
Convolutional
Encoder ...

Methods: The study
proposes
convolutional encoder
with 1/2 code rate and
constrained length of
3. An improved
architecture which
optimizes critical path
delay is proposed to
achieve higher

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speeds. The design is carried out in MATLAB. The simulation of convolutional proposed architecture is done using XILINX 14.1 and implementation is done using FPGA SPARATAN 3AN.

Design and
Implementation of
High Speed Viterbi

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Decoder ...

The convolutional encoder is based on a rate $1/2$ mother

convolutional code with constraint length $K = 7$ corresponding to 64 trellis states.

The input serial stream is encoded in two branch X and Y with the following polynomial: X output (171 octal) Y output

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(133 octal) Figure 2 reports the encoder architecture. Figure 2
DVB-S

Convolutional Encoder Architecture .
VHDL implementation of Convolutional Encoder . Figure 2 shows the classical architecture of a convolutional encoder.

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How to implement convolutional encoder in VHDL - Surf-VHDL
In telecommunication, a convolutional code is a type of error-correcting code that generates parity symbols via the sliding application of a boolean polynomial function to a data stream. The sliding application represents

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the 'convolution' of the encoder over the data, which gives rise to the term

'convolutional coding'.

The sliding nature of the convolutional codes facilitates trellis

...

Convolutional code -
Wikipedia

ABSTRACT: This
paper represents the

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SDR implementation of convolutional encoder and Viterbi decoder. In this paper there are two parts where one part is based on the VHDL simulation of encoder and decoder and second part is based on hardware, in which all these simulations are implemented on SDR (an FPGA). This

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paper has taken
random

Vol. 3, Issue 5, May
2014 SDR And

Implementation of ...

In this paper, a
modified FPGA
scheme for the
convolutional encoder
and Viterbi decoder
based on the IEEE
802.11a standards of
WLAN is presented in

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OFDM baseband processing systems.

The proposed design supports a generic, robust and configurable Viterbi decoder with constraint length of 7, code rate of $1/2$ and decoding depth of 36 symbols.

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Encoder ...

Design Simulation
and Implementation
Timing Results This
research presents the
implementation of
Convolutional
encoder- Viterbi
decoder architecture
on XC3S500E chip
[10], using
Spartan-3E FPGA
Starter Kit, Project
Navigator 8.2i

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Software (for modeling, verification and implementation) and Model Sim XE II/ Starter 5.8c Software which is used for timing simulation.

FPGA Based
Implementation of
Convolutional
Encoder ...

In order to simplify the hardware design and

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reduce the resource requirements, this paper proposes a novel implementation of a convolutional auto-encoder (CAE) in a field programmable gate array...

(PDF) An FPGA Implementation of a Convolutional Auto-Encoder

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126 FPGA Design and Implementation of a Convolutional Encoder and a Viterbi Decoder Based on 802.11a for OFDM development the VA operation problem has been solved to a great extent. This makes the Viterbi the most extensive, robust and capable decoding algorithm

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when the value of m is less than or equal to 10.

FPGA Design and Implementation of a Convolutional Encoder ...

Implementation of convolutional encoder and Viterbi decoder using VHDL Abstract: This work focuses on the realization of

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Implementation of convolutional encoder and adaptive Viterbi decoder (AVD) with a constraint length, K of 3 and a code rate (k/n) of $1/2$ using field-programmable gate array (FPGA) technology.

Implementation of convolutional encoder and Viterbi ...

Implementation Of

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Convolutional

Encoder And Viterbi

In this paper, a
modified FPGA

scheme for the

convolutional encoder
and Viterbi decoder

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processing systems.

The proposed design

supports a generic,

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robust and
configurable Viterbi
decoder with
constraint length of 7,
code rate of 1/2 and
decoding depth of 36
symbols.

FPGA Design and
Implementation of a
Convolutional
Encoder ...

A Convolutional
Encoder with 5-bit

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input and 2-bit output

The convolutional encoder is effectively a 5-bit shift register with bits

$[x_0, x_1, x_2, x_3, x_4]$

where x_0 is the new incoming bit and x_4 is the oldest bit in the register that is shifted out on each cycle. For PSK31 each bit will come in at 31.25Hz. Note, here is a post

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on Convolutional
Decoding.

PSK31 Convolutional
Encoder And
implementation in C
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